

## AMENDMENTS TO THE CLAIMS

### Listing Of Claims

1. (currently amended) A semiconductor component comprising:

a ~~metal~~ leadframe having a first surface and an opposing second surface, the leadframe comprising a plurality of leadfingers having tip portions configured to provide a die mounting site on the first surface, a plurality of terminal bonding sites on the tip portions on the second surface in an area array, a plurality of interconnect bonding sites on the first surface, and at least one bus bar on selected tip portions connecting selected terminal bonding sites;

a semiconductor die ~~having a back side attached to the die mounting site;~~

~~leadframe in a chip on board configuration;~~

a plurality of interconnects bonded to the die and to the interconnect bonding sites; and  
~~the leadframe; and~~

a plurality of terminal contacts attached to the terminal bonding sites.  
~~leadframe in an area array.~~

2. (original) The semiconductor component of claim 1 and further comprising an encapsulant encapsulating the die, the interconnects and the leadframe.

3. (original) The semiconductor component of claim 1 wherein the terminal contacts comprise bumps or balls in a grid array.

4. (original) The semiconductor component of claim 1 wherein the interconnects comprise wire bonded wires.

5. (currently amended) A semiconductor component comprising:

a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on a first side thereof, ~~and~~ a plurality of terminal bonding sites on a second side thereof in an area array, and at least one bus bar electrically connecting selected leadfingers;

a semiconductor die having a back side attached to the leadfingers on the first side and substantially covering the bus bar;

a plurality of interconnects bonded to the die and to the interconnect bonding sites;

a plurality of terminal contacts on the terminal bonding sites; and

an encapsulant encapsulating the die, the interconnects and the leadframe.

6. (currently amended) The semiconductor component of claim 5 further comprising ~~at least one~~ a plurality of bus bars substantially covered by the die.

~~electrically connecting selected leadfingers and located to not cross the interconnects.~~

7. (original) The semiconductor component of claim 5 wherein the interconnects comprise wire bonded wires.

8. (original) The semiconductor component of claim 5 wherein the terminal contacts comprise bumps or balls and the terminal bonding sites are arranged in a grid array.

9. (original) The semiconductor component of claim 5 wherein the leadframe comprises a chip on board leadframe.

10. (original) The semiconductor component of claim 5 further comprising an adhesive member attaching the back side of the die to the leadfingers.

11. (original) The semiconductor component of claim 5 wherein the interconnect bonding sites comprise first metal layers on the leadfingers.

12. (original) The semiconductor component of claim 5 wherein the terminal bonding sites comprise second metal layers on the leadfingers.

13. (original) The semiconductor component of claim 5 wherein the leadframe and the encapsulant have a chip scale outline.

14. (currently amended) A semiconductor component comprising:

- a leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on the leadfingers, a plurality of terminal bonding sites on the leadfingers in an area array, and at least one bus bar in the area array electrically connecting selected leadfingers;

- a semiconductor die comprising a circuit side, a plurality of die contacts on the circuit side, and a back side attached to the leadframe;

- a plurality of interconnects bonded to the die contacts and to the interconnect bonding sites;

- a plurality of terminal contacts on the terminal bonding sites; and

- an encapsulant encapsulating the die and the leadframe.

15. (original) The semiconductor component of claim 14 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bar is located proximate to an inner portion of the leadframe.

16. (original) The semiconductor component of claim 14 wherein the interconnect bonding sites are located relative to the bus bar such that the interconnects do not cross the bus bar.

17. (original) The semiconductor component of claim 14 wherein the interconnects comprise wire bonded wires.

18. (original) The semiconductor component of claim 14 wherein the terminal contacts comprise metal bumps or balls and the terminal bonding sites are arranged in a grid array.

19. (original) The semiconductor component of claim 14 wherein the interconnect bonding sites comprise first metal layers on a first side of the leadfingers and the terminal bonding sites comprise second metal layers on an opposing second side of the leadfingers.

20. (currently amended) A semiconductor component comprising:

a leadframe having a first side, an opposing second side, an inner portion and an outer periphery, the leadframe comprising a plurality of leadfingers and a plurality of bus bars proximate to the inner portion electrically connecting selected leadfingers;

a plurality of interconnect bonding sites on the leadfingers on the first side located proximate to the outer periphery;

a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array;

~~at least one bus bar electrically connecting selected leadfingers located proximate to the inner portion;~~

a semiconductor die back bonded to the leadfingers on the first side and substantially covering the bus bars;

a plurality of interconnects bonded to the die and to the interconnect bonding sites; and

a plurality of terminal contacts on the terminal bonding sites.

21. (original) The semiconductor component of claim 20 further comprising an encapsulant encapsulating the die and the leadframe.

22. (original) The semiconductor component of claim 20 wherein the leadframe has a chip on board configuration.

23. (currently amended) The semiconductor component of claim 20 wherein the interconnects comprise wires.

24. (original) The semiconductor component of claim 20 further comprising an adhesive member attaching the die to the first side.

25. (original) The semiconductor component of claim 20 wherein the terminal contacts comprise metal balls or metal bumps.

26. (original) The semiconductor component of claim 20 wherein the leadframe includes a die mounting site on the first side proximate to the inner portion.

27. (currently amended) A semiconductor component comprising:

a leadframe having a first side and an opposing second side, the leadframe comprising a plurality of leadfingers having tip portions configured to form a die mounting site on the first side, a plurality of interconnect bonding sites on the first side outside of the die mounting site, a plurality of terminal bonding sites on the second side in

an area array and a plurality of bus bars on selected tip portions electrically connecting selected leadfingers;

a semiconductor die having a back side attached to the die mounting site;

a plurality of interconnects bonded to the die and to the interconnect bonding sites, the interconnect bonding sites and the bus bars located on the leadframe such that the interconnects do not cross the bus bars;

a plurality of terminal contacts on the terminal bonding sites; and

an encapsulant encapsulating the die, the leadframe, and the interconnects.

28. (original) The semiconductor component of claim 27 wherein the interconnect bonding sites are located proximate to an outer periphery of the leadframe and the bus bars are located proximate to an inner portion of the leadframe.

29. (original) The semiconductor component of claim 27 wherein the leadfingers are arranged in rows along opposing sides of the leadframe.

30. (original) The semiconductor component of claim 27 wherein the interconnects comprise wires.

31. (original) The semiconductor component of claim 27 wherein the leadframe has a chip on board configuration.

32. (original) The semiconductor component of claim 27 wherein the encapsulant has a chip scale outline.

33. (original) The semiconductor component of claim 27 wherein the leadframe has a chip scale outline.

34. (original) The semiconductor component of claim 27 wherein the interconnect bonding sites and the terminal bonding sites comprise a metal selected from the group consisting of Al, Cu, Au and alloys thereof.

35. (original) The semiconductor component of claim 27 wherein the die comprises a plurality of die contacts on the circuit side and the interconnects are bonded to the die contacts.

36. (original) The semiconductor component of claim 27 wherein the terminal contacts comprise bumps or balls in a grid array.

Claims 37-63 (canceled)

64. (currently amended) A system comprising:

a substrate; and

a semiconductor component on the substrate comprising a ~~chip on board~~ leadframe comprising a plurality of leadfingers, a plurality of interconnect bonding sites on a first surface of the leadfingers, and a plurality of terminal bonding sites on an opposing second surface of the leadfingers in an area array, at least one bus bar electrically connecting selected leadfingers, a semiconductor die back bonded to the leadfingers substantially covering the bus bar, a plurality of interconnects bonded to the die and to the interconnect bonding sites, a plurality of terminal contacts on the terminal bonding sites, and an encapsulant encapsulating the die, the interconnects and the leadframe.

65. (original) The system of claim 64 wherein the substrate comprises a module substrate and the system comprises a multi chip module.

66. (original) The system of claim 64 wherein the substrate is contained in a computer.

67. (original) The system of claim 64 wherein the substrate is contained in a camcorder.

68. (original) The system of claim 64 wherein the substrate is contained in a camera.

69. (original) The system of claim 64 wherein the substrate is contained in a cell phone.

70. (currently amended) A system comprising:  
a substrate comprising a plurality of electrodes; and  
a semiconductor component on the substrate comprising:  
a leadframe having a first side, an opposing second side, an inner portion and an outer periphery, the leadframe comprising a plurality of leadfingers;  
a plurality of interconnect bonding sites on the leadfingers on the first side located proximate to the outer periphery;  
a plurality of terminal bonding sites on the leadfingers on the opposing second side in an area array;  
at least one bus bar in the area array electrically connecting selected leadfingers located proximate to the inner portion;  
a semiconductor die back bonded to the leadfingers on the first side substantially covering the bus bar;



a plurality of interconnects bonded to the die and to the interconnect bonding sites; and

a plurality of terminal contacts on the terminal bonding sites bonded to the electrodes on the substrate.

71. (original) The system of claim 70 wherein the system comprises a multi chip module, a computer, a camcorder, a camera or a cell phone.

72. (original) The system of claim 70 wherein the terminal contacts comprise metal bumps or balls.

73. (original) The system of claim 70 wherein the leadframe has a chip on board configuration.

74. (original) The system of claim 70 wherein the interconnects comprise wire bonded wires.

75. (original) The system of claim 70 wherein the component has a chip scale outline.